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EXAMINER	
SWERDLOW, DANIEL	

ART UNIT	PAPER NUMBER
2644	

DATE MAILED: 01/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,159	CASPER, BRYAN K.	
	Examiner	Art Unit	
	Daniel Swerdlow	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7-20* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/02, 9/10/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Due to an apparent typographical error, Claim 20, as presented, depends from Claim 16. It is clear that applicant intended that Claim 20 depend from Claim 18. Because of the error, there are numerous instances of lack of antecedent basis in the claim. In order to advance prosecution to the maximum degree possible, examiner makes prior art rejections below based on the interpretation that applicant intended Claim 20 to depend from Claim 18.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Cecchi et al. (US Patent 6,344,756).

5. Regarding Claim 1, Cecchi '756 discloses an echo cancellation circuit with a comparator (Fig. 1, reference 112; column 3, lines 38-52) that has an input (Fig. 1, reference 118, 120) to receive a signal from a bus cable (i.e., a transmission line analog signal level) and receives a

replica driver output (i.e., a substantially variable offset) that is a scaled copy of a transmit signal (i.e., controllable to represent a variable offset level) (Fig. 1, reference 122, 124; column 3, lines 43-45) and is subtracted from the transmission line signal (i.e., the comparator provides an output value that represents a comparison between the transmission line analog signal and the variable reference level) (column 3, lines 48-50).

6. Claim 8 is essentially similar to Claim 1 and is rejected on the same grounds.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 2 through 4, 7 and 9 through 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cecchi '756 in view of Cecchi (US Patent 6,304,106) and further in view of Lee et al. (IEEE Journal of Solid State Circuits).

9. Regarding Claim 2, Cecchi '756 further discloses a driver (Fig. 1, reference 102; column 3, lines 2-5) that drives output signals to a bus cable (i.e., coupled to transmit driver data symbols). Further it is clear from Fig. 2 of US Patent 6,304,106 to Cecchi et al. which is incorporated by reference in Cecchi '756 and the associated description (Cecchi '106: Column 2, line 63 through column 3, line 18) that includes gates and pin connections that the driver and echo cancellation circuit are on the same integrated circuit die. Further, Cecchi '756 discloses a

replica driver (Fig. 1, reference 104; column 3, lines 43-45) that shares an input with the driver (i.e., whose input is coupled to receive the driver data symbols) and whose output is subtracted from the transmission line signal by the comparator (i.e., is coupled to an offset control input of the comparator) (column 3, lines 48-50). Therefore, Cecchi '756 discloses all elements of Claim 2 except a discrete time echo cancellation filter. Cecchi '756 further discloses that the echo canceller therein must be customized for a given physical configuration (column 4, lines 19-21). As such, one skilled in the art would have been motivated to seek an echo canceller that did not need to be pre-customized for a particular physical configuration. Lee discloses a discrete time echo canceller for use at gigabit data rates in CMOS technology (abstract). Lee further discloses that the echo canceller adapts to cable length and impedance discontinuities (abstract). It would have been obvious to one skilled in the art at the time of the invention to apply the adaptive discrete time echo canceling taught by Lee to the circuit taught by Cecchi for the purpose of reducing cost and saving time by obviating the need for pre-customizing the echo canceller.

10. Regarding Claim 3, Lee further discloses the discrete time echo canceller using an LMS algorithm (i.e., a digital finite impulse response filter) (abstract; Fig. 5) with an output (Fig 5, to m1-m4) coupled (via multipliers m1-m4) to DAC1-DAC4 and a pair of summers that together correspond to the comparator claimed where the inputs to the DACs correspond to the offset control input to the comparator claimed.

11. Regarding Claim 4, as stated above, apropos of Claim 3, the inputs to the DACs in Fig. 5 in Lee correspond to the offset control input to the comparator claimed. As such this input is a digital input that receives a binary value.

12. Regarding Claim 7, Cecchi further discloses transmitting and receiving on the same transmission line (Fig. 1, reference 106; column 3, lines 38-41).

13. Claims 9 is essentially similar to Claim 2 and is rejected on the same grounds.

14. Regarding Claim 10, Lee further discloses training the filter by transmitting a sequence of steps (i.e., a training pattern of data signals) (p. 367, first full paragraph of second column) that are detected by the summer that corresponds to the comparator claimed and used to identify four significant taps (i.e., determining a plurality of coefficients) to vary an estimated echo (i.e., an offset to the comparator) to cancel echo (i.e., increase voltage margin of the near end receiver).

15. Regarding Claim 11, Lee further discloses subtraction of the transmitted signal from the transmitted+received signal (i.e., the outbound wave is subtracted from the transmission line signal) (Fig. 5, VIC1; p. 367, paragraph spanning columns) where VIC1, along with the summer, forms a part of the comparator claimed.

16. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cecchi '756 in view of Lee et al. (IEEE Journal of Solid State Circuits).

17. Regarding Claim 5, as shown above apropos of Claim 1, Cecchi '756 discloses all elements except a sample and hold circuit whose output is coupled to provide the transmission line analog signal level to the comparator. Cecchi '756 further discloses that the echo canceller therein must be customized for a given physical configuration (column 4, lines 19-21). As such, one skilled in the art would have been motivated to seek an echo canceller that did not need to be pre-customized for a particular physical configuration. Lee discloses a discrete time echo canceller for use at gigabit data rates in CMOS technology (abstract). Lee further discloses that

the echo canceller adapts to cable length and impedance discontinuities (abstract). In addition, the discrete time echo canceller disclosed by Lee uses a FIFO register (i.e., a sample and hold circuit) between the data input (i.e., the transmission line analog signal level) and the summer that corresponds to the comparator claimed. It would have been obvious to one skilled in the art at the time of the invention to apply the adaptive discrete time echo canceling including the FIFO register as taught by Lee to the circuit taught by Cecchi for the purpose of reducing cost and saving time by obviating the need for pre-customizing the echo canceller.

18. Claim 12 is essentially similar to Claim 5 and is rejected on the same grounds.

19. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cecchi '756 in view of Cecchi '756 and further in view of admitted prior art.

20. Regarding Claim 13, as shown above apropos of Claim 1, Cecchi '756 discloses all elements except the echo cancellation circuit being part of a bus receiver in an I/O section of an IC chip in a package installed on a printed wiring board on which a parallel bus is formed. Further it is clear from Fig. 2 of Cecchi '106 which is incorporated by reference in Cecchi '756 and the associated description (Cecchi '106: Column 2, line 63 through column 3, line 18) that includes gates and pin connections that the driver and echo cancellation circuit are part of a bus receiver in an I/O section of an IC chip in a package. As such, the combination of Cecchi '756 and Cecchi '106 meets all elements of Claim 13 except the IC package being installed on a printed wiring board on which a parallel bus is formed. Applicant admits as prior art the use of chips in separate IC packages with I/O circuits including drivers and receivers communicating over parallel busses on printed wiring board (paragraph 0002). It would have been obvious to

one skilled in the art at the time of the invention to apply the use of chips in separate IC packages with I/O circuits including drivers and receivers communicating over parallel busses on printed wiring board that applicant admits as prior art to the circuit disclosed by Cecchi for the purpose of utilizing the IC's in an interconnected system.

21. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cecchi '756 in view of Cecchi '106 and further in view of admitted prior art and further in view of Roy et al. (US Patent 6,388,495).

22. Regarding Claim 14, as shown above apropos of Claim 13, the combination of Cecchi '756, Cecchi '106 and admitted prior art makes obvious all elements except the integrated circuit having a microprocessor logic function. Roy discloses the combining of a CPU (i.e., microprocessor) logic function with a bus I/O function on a chip (Fig 1, reference 10; column 2, line 48-56; column 6, lines 14-19). It would have been obvious to one skilled in the art at the time of the invention to apply the CPU logic function as taught by Roy to the IC with I/O functions made obvious by Cecchi '756, Cecchi '106 and admitted prior art for the purpose of providing a CPU function to a computer system.

23. Regarding Claim 15, as shown above apropos of Claim 13, the combination of Cecchi '756, Cecchi '106 and admitted prior art makes obvious all elements except the integrated circuit having a microprocessor logic function. Roy discloses the combining of a memory logic function with a bus I/O function on a chip (Fig 1, reference 10; column 2, line 48-56; column 6, lines 14-19). It would have been obvious to one skilled in the art at the time of the invention to apply the memory logic function as taught by Roy to the IC with I/O functions made obvious by

Cecchi '756, Cecchi '106 and admitted prior art for the purpose of providing a memory function to a computer system.

24. Claims 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cecchi '756 in view of Cecchi '106 and further in view of admitted prior art and further in view of Chan et al. (US Patent 6,226,237).

25. Regarding Claim 16, as shown above apropos of Claim 13, the combination of Cecchi '756, Cecchi '106 and admitted prior art makes obvious all elements except the integrated circuit having a bus bridge logic function. Chan discloses an IC with a bus bridge logic function that inherently has a bus I/O function (Fig 1, reference 124; column 5, line 38-40). It would have been obvious to one skilled in the art at the time of the invention to combine the bus bridge logic function as taught by Chan to the IC with I/O functions made obvious by Cecchi '756, Cecchi '106 and admitted prior art for the purpose of providing a bus bridge function to a computer system.

26. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cecchi '756 in view of Cecchi '106 and further in view of admitted prior art and further in view of Lee.

27. Regarding Claim 17, Cecchi '756 further discloses a driver (Fig. 1, reference 102; column 3, lines 2-5) that drives output signals to a bus cable (i.e., coupled to transmit driver data symbols). Further it is clear from Fig. 2 of Cecchi '106, which is incorporated by reference in Cecchi '756 and the associated description (Cecchi '106: Column 2, line 63 through column 3, line 18) that includes gates and pin connections that the driver and echo cancellation circuit are

on the same integrated circuit die. Further, Cecchi '756 discloses a replica driver (Fig. 1, reference 104; column 3, lines 43-45) that shares an input with the driver (i.e., whose input is coupled to receive the driver data symbols) and whose output is subtracted from the transmission line signal by the comparator (i.e., is coupled to an offset control input of the comparator) (column 3, lines 48-50). Therefore, Cecchi '756 and admitted prior art make obvious all elements of Claim 17 except a discrete time echo cancellation filter. Cecchi '756 further discloses that the echo canceller therein must be customized for a given physical configuration (column 4, lines 19-21). As such, one skilled in the art would have been motivated to seek an echo canceller that did not need to be pre-customized for a particular physical configuration. Lee discloses a discrete time echo canceller for use at gigabit data rates in CMOS technology (abstract). Lee further discloses that the echo canceller adapts to cable length and impedance discontinuities (abstract). It would have been obvious to one skilled in the art at the time of the invention to apply the adaptive discrete time echo canceling taught by Lee to the circuit taught by Cecchi for the purpose of reducing cost and saving time by obviating the need for pre-customizing the echo canceller.

28. Claims 18 through 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe et al. (US Patent 4,651,284).

29. Regarding Claim 18, Watanabe discloses a system including a CPU (i.e., processor) (Fig. 15, reference 41; column 9 lines 55-61) that displays a layout (i.e., representation) of an electronic circuit from a database (i.e., instructions) on a magnetic disk file (i.e., a machine readable medium). Watanabe does not expressly show an echo cancellation circuit in which a

comparator has an input to receive a transmission line analog signal level, the comparator having a substantially variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the transmission line analog signal level and the variable reference level. However these differences are only found in the nonfunctional data stored on the article of manufacture. An echo cancellation circuit in which a comparator has an input to receive a transmission line analog signal level, the comparator having a substantially variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the transmission line analog signal level and the variable reference level is not functionally related to the substrate of the article of manufacture. Thus, this descriptive material will not distinguish the claimed invention from the prior art in terms of patentability, see In re Gulack, 703 F.2d 1381, 1385, 217 USPQ 401, 404 (Fed. Cir. 1983); In re Lowry, 32 F.3d 1579, 32 USPQ2d 1031 (Fed. Cir. 1994). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to store instructions for the representation of any circuit in the article of manufacture as shown in Watanabe because such instructions do not functionally relate to the substrate of the article of manufacture. See Gulack cited above.

30. The additional limitations of Claims 19 and 20 are directed solely to nonfunctional data on the article of manufacture. As such, Claims 19 and 20 are rejected for reasons stated above apropos of Claim 18.

31. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Cecchi '756.

32. Regarding Claim 18, Watanabe discloses a system including a CPU (i.e., processor) (Fig. 15, reference 41; column 9 lines 55-61) that displays a layout (i.e., representation) of an electronic circuit from a database (i.e., instructions) on a magnetic disk file (i.e., a machine readable medium). Watanabe does not expressly show an echo cancellation circuit in which a comparator has an input to receive a transmission line analog signal level, the comparator having a substantially variable offset that is controllable to represent a variable reference level, an output of the comparator to provide a value that represents a comparison between the transmission line analog signal level and the variable reference level. As shown above apropos of Claim 1, Cecchi '756 discloses the structural limitations of the echo canceller circuit. Watanabe discloses that the system solves problems involving circuit layout and provides other advantages (column 3, lines 8-46). It would have been obvious to one skilled in the art at the time of the invention to combine the system taught by Watanabe and the echo canceller circuit taught by Cecchi '756 for the purpose of realizing the aforesaid advantages.

33. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Cecchi '756 and further in view of Cecchi '106 and further in view of Lee.

34. As shown above apropos of Claim 2 the additional limitations of Claim 19 are made obvious by the combination of Cecchi '756, Cecchi '106 and Lee. It would have been obvious to one skilled in the art at the time of the invention to combine the system taught by Watanabe and

the combination made obvious by Cecchi '756, Cecchi '106 and Lee for the purpose of realizing the advantages stated above apropos of Claim 18.

Allowable Subject Matter

35. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

36. The following is a statement of reasons for the indication of allowable subject matter:

37. As shown above apropos of Claim 1, Cecchi '756 anticipates all elements except for the structural details of the comparator. Tanji (US Patent 6,201,443) discloses a variable gain amplifier that corresponds to the comparator claimed. However, Tanji does not disclose or fairly suggest intentionally unbalanced transistor pairs as claimed. Therefore, Claim 6 is allowable matter.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Swerdlow whose telephone number is 703-305-4088. The examiner can normally be reached on Monday through Friday between 8:00 AM and 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curtis A. Kuntz can be reached on 703-305-4708. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Daniel Swerdlow, Patent Examiner Art Unit 2644